MARVELL

Enabling AI Silicon Solutions for Next Generation Data Infrastructure

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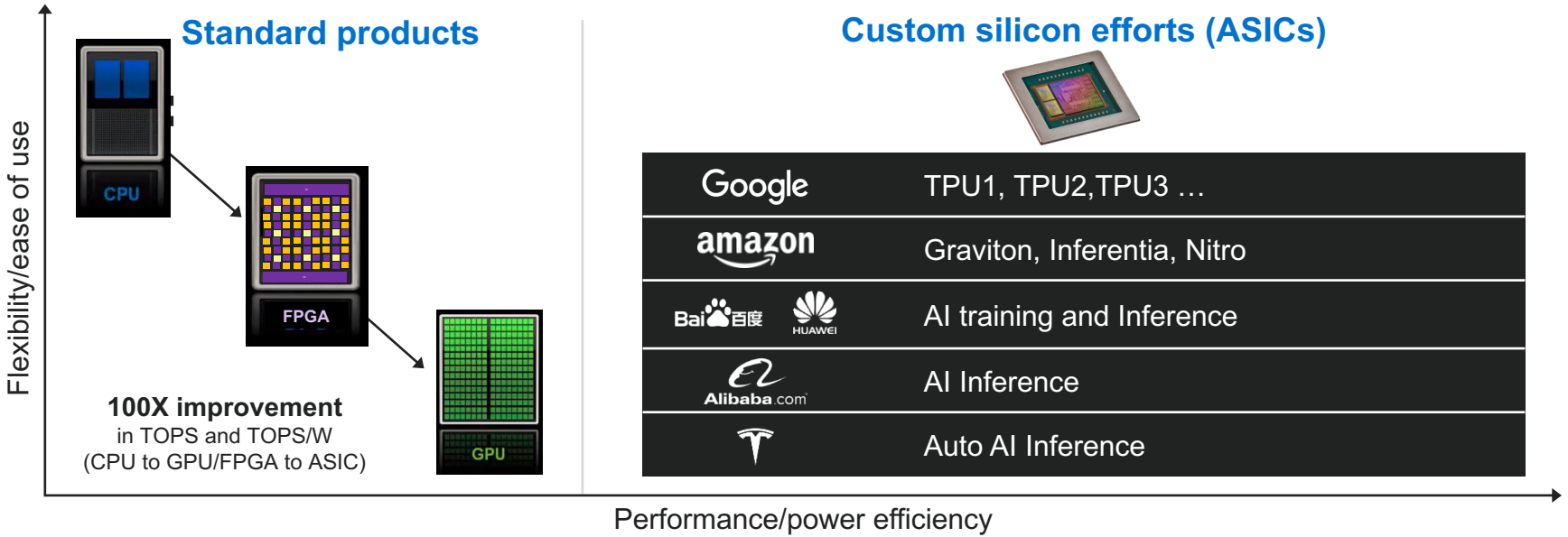
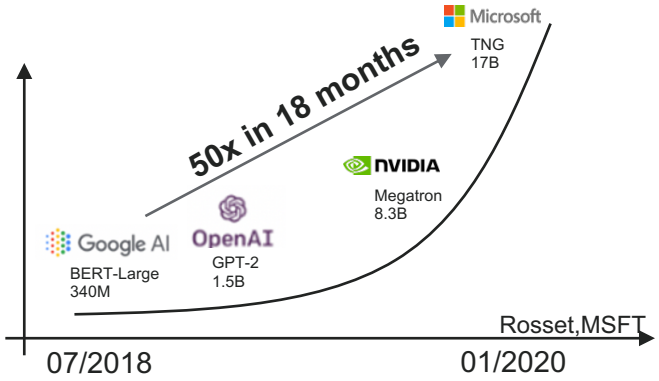
Industry trend:
Custom AI silicon needed for data infrastructure



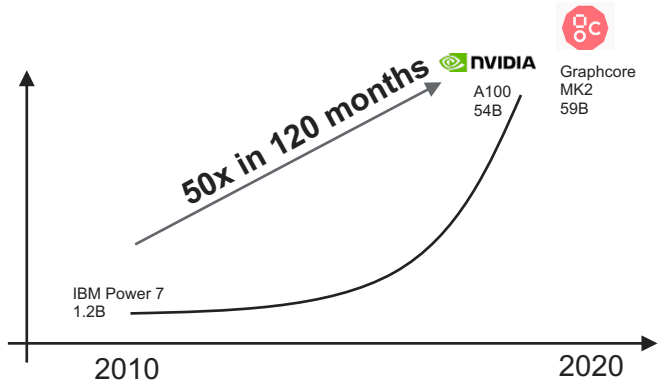
Higher-performance at a lower energy per operation
Quality and reliability critical

Industry trend:
Growing AI models to silicon scaling gap

AI model growth



Moore's law scaling (transistors/die)



AI models doubling every 3.5 months	Logic/chip doubling every >18 months	SRAM/chip doubling every > 48 months

Marvell ASIC Introduction

Established ASIC business - spanning

14 process nodes

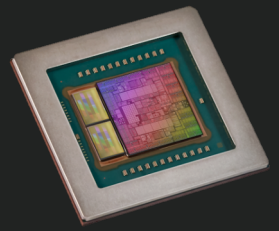
Over 2000 designs

with record first pass successes

Leading-edge IPs

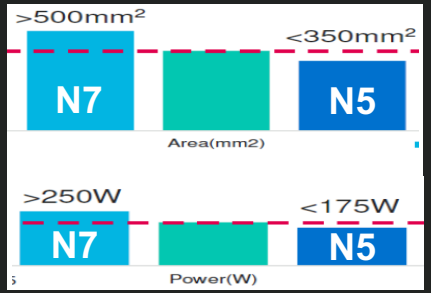
Design Services

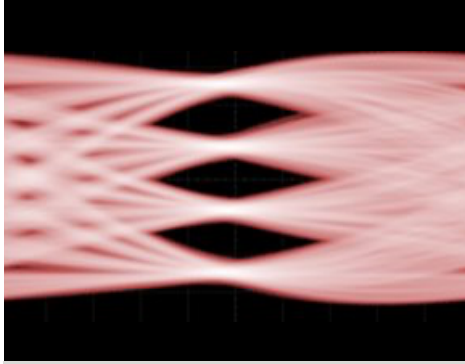
Advanced Packaging Technologies



Marvell offers

the best of breed



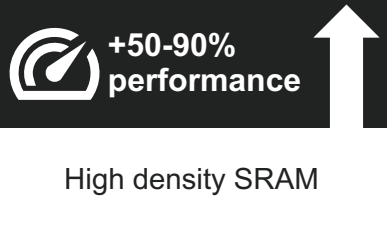


Leading-edge technology

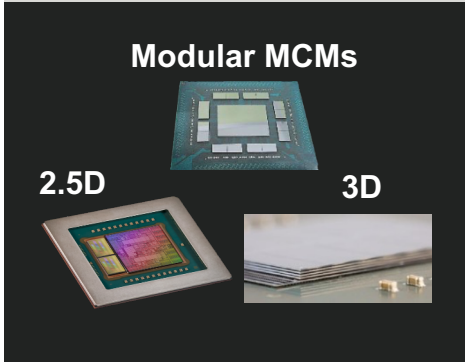
Best in class IO

Highest performance
112G and parallel IOs

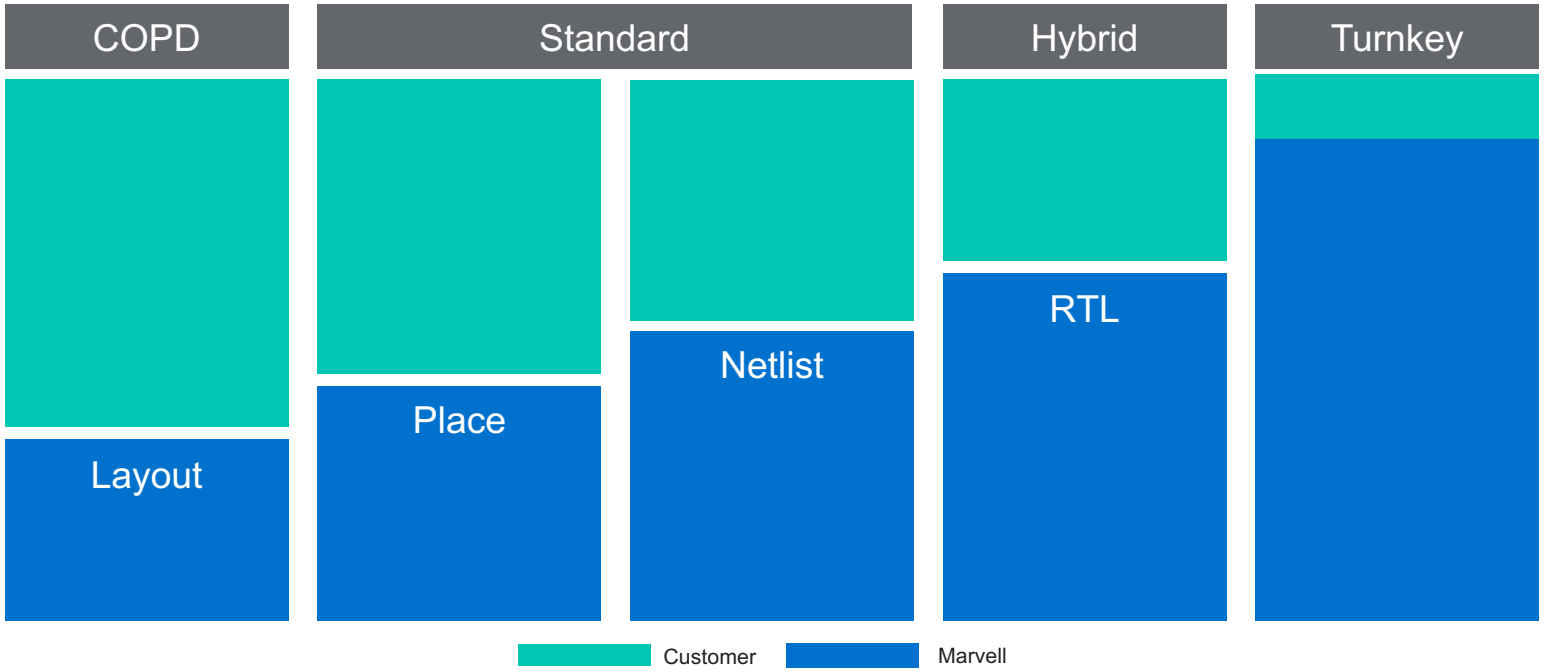
Highest bandwidth SRAM



Advanced packaging



Flexible custom ASIC engagement business models



Close collaboration from design architecture start to tapeout release

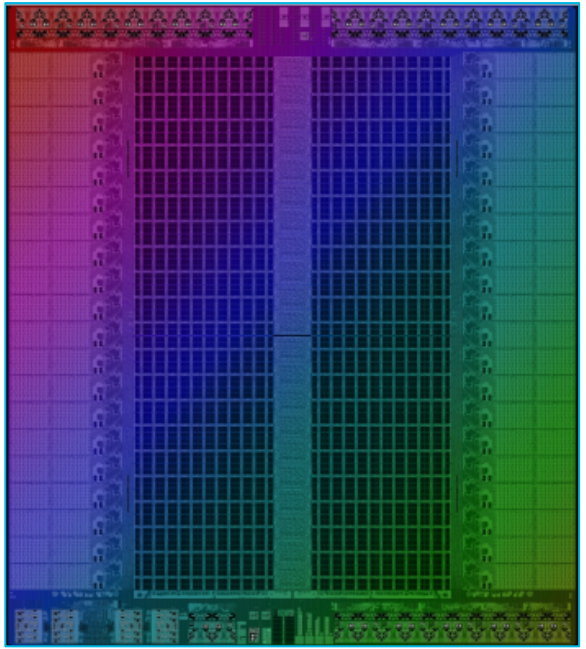
Marvell enables Groq's 1st PetaOPs AI accelerator

First-time-right 700+mm2 custom ASIC in volume production

Groq architectural innovations:
High-performance and low latency
Multi-chip scalability with deterministic execution

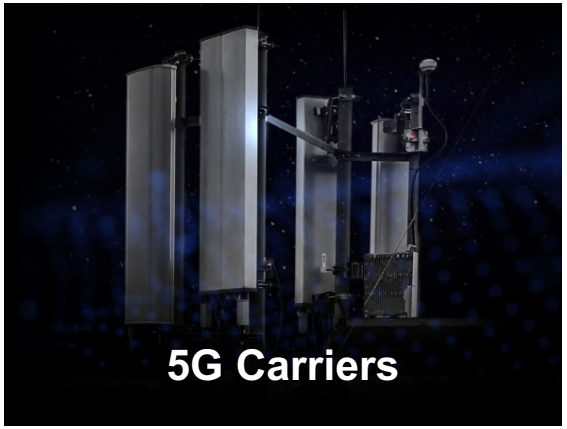
Best-in-class Marvell IPs:
High-speed SerDes
Dense SRAM
Full turnkey PCIe & C2C subsystems

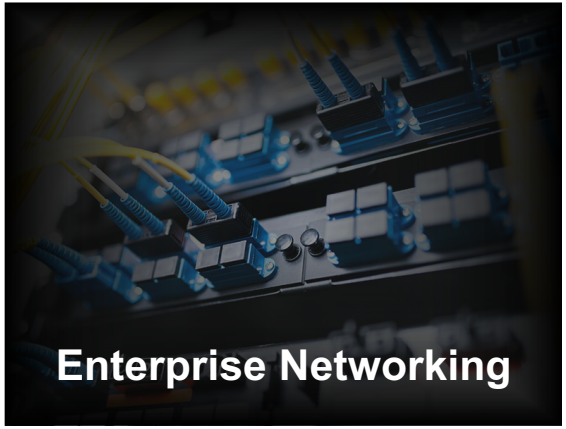
Reliability enhancements for 99.999% availability:
Pre-qualified IP and design flow
Custom test, logic redundancy and ECC
Reliability support from netlist to end-of-life



Final netlist to tape-out in < 3months

Enabling custom data infrastructure silicon solutions





Marvell offers

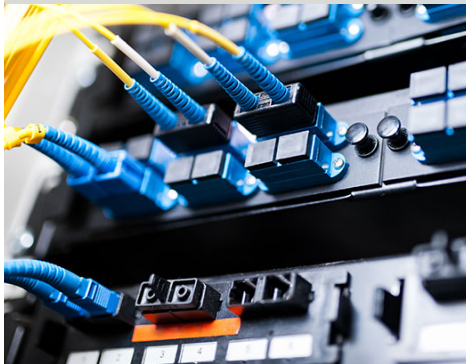
the most complete data infrastructure portfolio

Processors
#1 in baseband and data plane processors

Storage
#1 in HDD, SSD and Fibre Channel controllers

Networking
#2 in Switches and PHYs

Security
#1 in security processors



Custom silicon for data centers

Building blocks

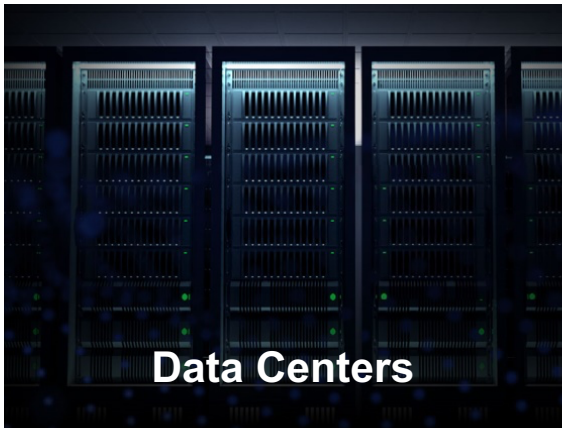
- Optimized 112G+ SerDes / HBM
- Machine learning optimized memory
- High-perf. custom ARM processors
- Programmable Logic
- Switch / Routing IP
- Encryption / Decryption
- Compression/Decompression
- RDMA / iWarp / Network Offload

Custom silicon

- On package memory
- Chiplet Based Accelerators

AI accelerators

Smart NICs



Reliability and uptime 99.999%

Custom silicon for computational storage

Building blocks

NAND Media Controller

DSP and LDPC ECC

Encryption / Data Protection

High-performance custom ARM processors

Programmable Logic

CXL / PCIe / NVMe

FTL

Firmware

Storage capability
IP / subsystems / firmware

On package memory

Chiplet based accelerators

Custom silicon

LPDDR

PCIe NVMe

CPU

AI / ML

DDR or SCM

Computational SSD

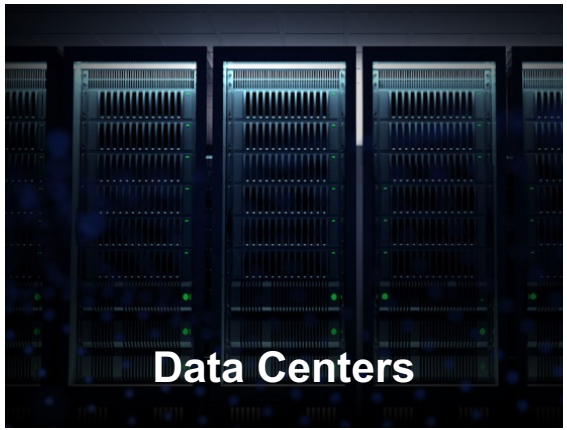
SiP

Ser Des

CXL

DDR or SCM

Disaggregated memory



Reliability and uptime 99.999%

Custom silicon for automotive

Building blocks

Secure PHY / Switch / CNTLs

NVMe / NVMeOF

High-performance multi-core ARM processors solutions

Security IP

Safety Island / Safety Monitors

Proven Interface IP

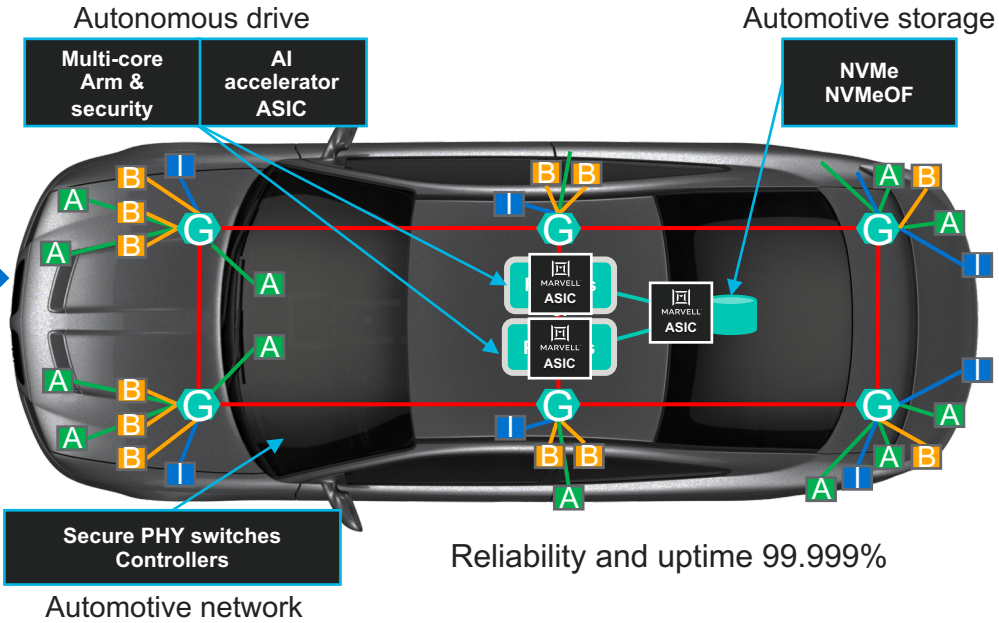
High-bandwidth SRAM / LD / GD

On package memory

Chiplet based accelerators

Full turnkey capability

Custom silicon



Reliability and uptime 99.999%

Proactive measures to maintain reliability & availability

FAB & OSAT partnerships	Deep understanding of technology intrinsic failure mechanisms Design for reliability
IP design methodology	Pre-qualified internal and 3rd party IP
Chip design methodology	Pre-qualified chip design methodology
Image/package (qualified chip carrier)	Pre-qualified image / package offering
Test (module that works as models predict for supported lifetime)	Pre-qualified reliability and quality screens from qualification test vehicles Enhanced escape prevention methodology for Automotive and Aerospace

Summary: Marvell's unique custom silicon offering

1. Industry's only complete data infrastructure IP portfolio
2. 25-year custom ASIC track record of execution with >2000 high-reliability production ASICs
3. Shipping multiple AI/ML ASICs including PetaOP/s accelerators
   Scaling to advanced technology nodes with 5nm hardware in the lab
4. Offering industry's most flexible business models to enable next generation innovations

MARVELL

Thank You

Essential technology, done right™