

Marvell® AQC111C & AQC112C Ethernet Controllers

5 GbE & 2.5 GbE PCIe AQtion Multi-Gigabit Ethernet Controller

Overview

The Marvell® AQtion AQC111C 5G and the AQC112C 2.5G are high-performance, Multi-Gig Ethernet controllers housed in a compact 9 mm x 9 mm package. Their ultra-small footprint and low-cost design makes these controllers the perfect solution for PCIe LAN on Motherboard (LOM) implementations as well as other embedded platforms. By offering Multi-Gig Ethernet speeds up of 5 GbE and 2.5 GbE, Marvell AQtion AQC111C and AQC112C controllers offer flexible design options for OEMs of desktop workstations, mass-market PCs and motherboards looking to offer a seamless, Multi-Gig upgrade path to their customers.

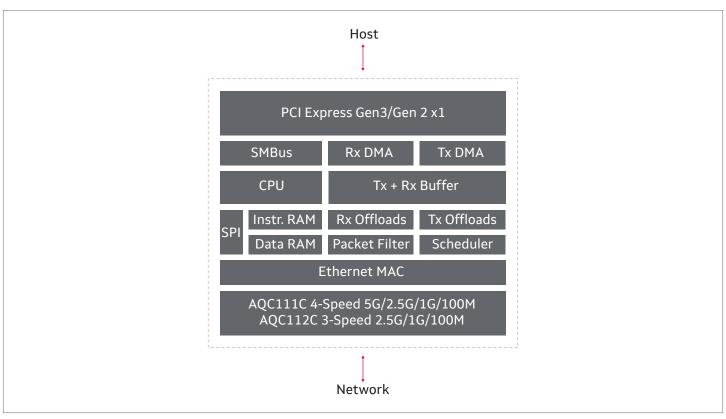
End-users will benefit from the out-of-the-box Multi-Gig experience, without the need to upgrade, and can easily maximize the benefit of the existing Cat 5e cabling that is commonly found in most buildings.

With support for PCI Express Gen3/Gen2 x1, this new AQtion architecture easily handles up to 5 GbE line-rate performance. Both the AQC111C and the AQC112C incorporate the industry proven Marvell AQrate PHY technology which delivers 5 GbE and 2.5 GbE network connectivity speed through 100 meters of the Cat 5e cabling.

The AQC111C controller supports both 5 and 2.5 Multi-Gig Ethernet over copper, or 5/2.5GBASE-T, and is compliant with the IEEE 802.3an/bz standard, as well as the NBASE-T Alliance PHY specification.

All AQtion controllers are backward-compatible with legacy 1000BASE-T Ethernet or Gigabit Ethernet. The AQC111C and AQC112C are also backward compatible to support 100Mb Ethernet. Both controllers integrate Energy Efficient Ethernet (EEE), and delivers wire-speed performance at all supported rates.

Block Diagram



Key Features

Features	Benefits	
Single-chip solution	 Integrated PCIe, MAC, and PHY minimizes board space and power utilization 	
PCI Express Gen3/Gen2	Supports line rate of up to 8.0 GT/s per lane	
Bus width	· Supports Gen3/Gen2 x1	
MSI, MSI-X, and legacy INTx PCIe interrupts	Improves CPU utilization and network performance	
Two SMBus (Master/Slave + Slave)	Supports communication and management function	
PHY Specific Features	Benefits	
Integrated Marvell AQrate PHY featuring NBASE-T technology	 100 meters over Cat 5e or better at 5 Gbps, 2.5 Gbps, 1 Gbps, 100 Mbps (requires no change to existing infrastructure or cabling) 	
Advanced cable diagnostics	On-chip high resolution cable analyzer	
Audio Video Bridging (AVB) and PTP/1588v2	Management of time-sensitive traffic packets	
MAC Specific Features	Benefits	
 Large Send Offload (LSO) Receive Side Scaling (RSS) Direct Cache Access (DCA) Header checksum 	Increased network performance and lower host CPU utilization	
Receive Side Scaling (RSS)Direct Cache Access (DCA)	 Increased network performance and lower host CPU utilization Supports lower power modes 	
 Receive Side Scaling (RSS) Direct Cache Access (DCA) Header checksum 		
 Receive Side Scaling (RSS) Direct Cache Access (DCA) Header checksum Wake-on-LAN (WoL) power management	Supports lower power modes	
 Receive Side Scaling (RSS) Direct Cache Access (DCA) Header checksum Wake-on-LAN (WoL) power management On-chip CPU DASH	Supports lower power modesDesktop management	
 Receive Side Scaling (RSS) Direct Cache Access (DCA) Header checksum Wake-on-LAN (WoL) power management On-chip CPU DASH Internet Control Message Protocol (ICMP) 	 Supports lower power modes Desktop management Supports diagnostic, error, and operational information messages 	
 Receive Side Scaling (RSS) Direct Cache Access (DCA) Header checksum Wake-on-LAN (WoL) power management On-chip CPU DASH Internet Control Message Protocol (ICMP) Address Resolution Protocol (ARP) 	 Supports lower power modes Desktop management Supports diagnostic, error, and operational information messages Resolves network layer addresses into link layer addresses 	
 Receive Side Scaling (RSS) Direct Cache Access (DCA) Header checksum Wake-on-LAN (WoL) power management On-chip CPU DASH Internet Control Message Protocol (ICMP) Address Resolution Protocol (ARP) Multicast Domain Name System (mDNS) 	 Supports lower power modes Desktop management Supports diagnostic, error, and operational information messages Resolves network layer addresses into link layer addresses Resolves host names to IP addresses 	
 Receive Side Scaling (RSS) Direct Cache Access (DCA) Header checksum Wake-on-LAN (WoL) power management On-chip CPU DASH Internet Control Message Protocol (ICMP) Address Resolution Protocol (ARP) Multicast Domain Name System (mDNS) Transmission Control Protocol (TCP) Keepalives (KA) 	 Supports lower power modes Desktop management Supports diagnostic, error, and operational information messages Resolves network layer addresses into link layer addresses Resolves host names to IP addresses Supports link checking between devices 	

Ordering Codes

Part Number	Speed	Package
AQC111C	4-Speed	9 mm x 9 mm
AQC112C	3-Speed	9 mm x 9 mm

This AQtion device is in a 9 mm x 9 mm, 0.8 mm pitch 100-pin FCBGA

Target Applications

Motherboards, PCs, Workstations, docking stations, NAS, Routers, Gateways, and other embedded applications.

Drivers: Windows 10 (32-bit/64-bit), Windows 8.0/8.1 (32-bit/64-bit), Windows 7 (32-bit/64-bit), Linux 3.10 and higher

Utilities: ROM programming and Windows installer

Boot Options: UEFI and PXE

