Alaska® P Gen6 16L PCIe Retimer

Low-power, low-latency, 16-lane PCIe Gen 6/CXL 3 protocol-aware retimer
P/N MV-CHP10160

Overview

The Alaska® P Gen6 16L PCIe Retimer (MV-CHP10160) is a 16-lane, low-power, low-latency, fully PCI Express® Gen 6.x-compliant device with leading I/O performance. It is capable of driving sixteen lanes of maximum 64 Gbps signal, extending the reach between PCIe root complex (RC) and end point (EP).

The MV-CHP10160 is optimized for low-latency applications with Compute Express Link™ 3.x protocol and its long-range SerDes on both sides (upstream and downstream) support transmission over high-loss channels.

The MV-CHP10160 can operate at 64 GT/s, 32 GT/s, 16 GT/s, 8 GT/s, 5 GT/s, and 2.5 GT/s PCIe Data Rate with automatic link equalization and training per PCIe specifications.
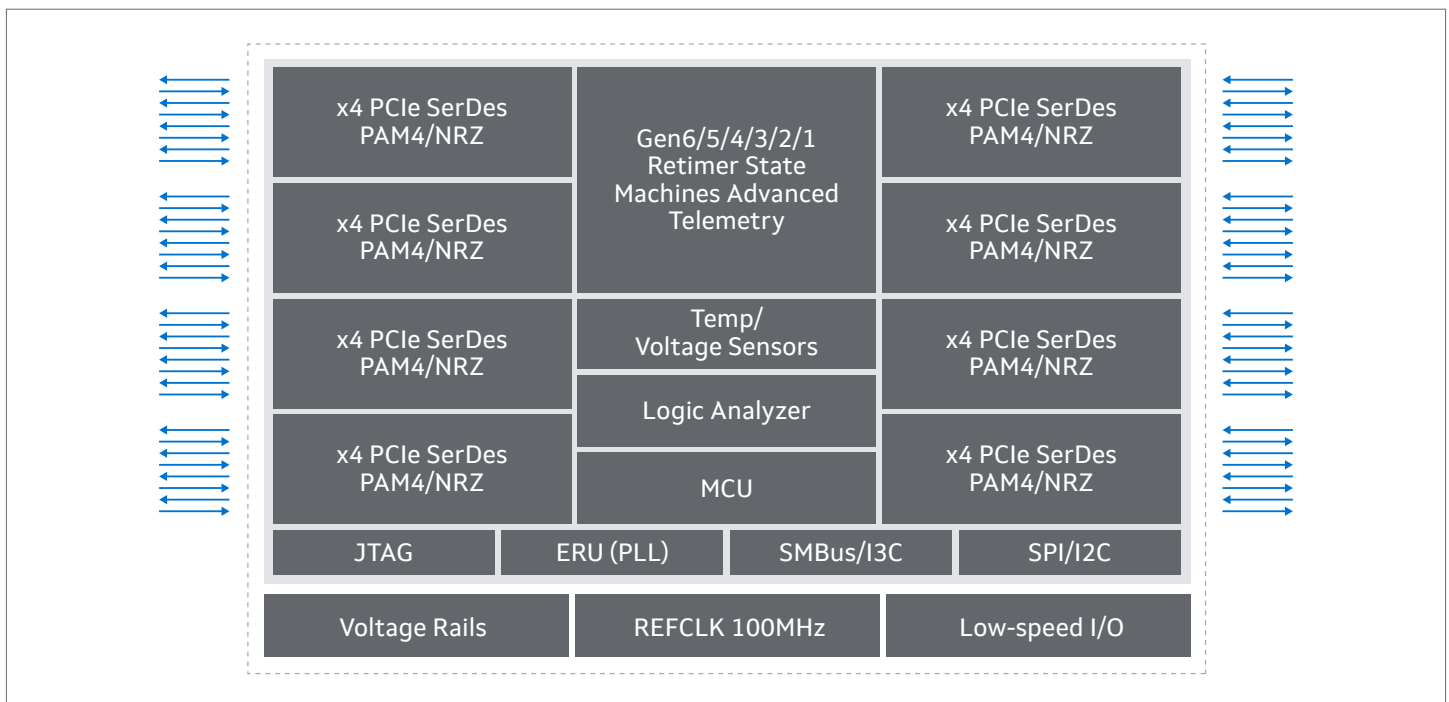
The MV-CHP10160 exceeds PCI-SIG electrical specifications with >32 dB Insertion Loss (IL) at 64 GT/s (PCIe 6) and >36 dB IL at 32 GT/s (PCIe 5). The device enables customers to scale compute fabric inside accelerated systems, general-purpose servers, and cache-coherent disaggregated infrastructure.

The MV-CHP10160 follows Intel PCIe 6.0 Retimer Supplemental Footprint and enables gen-to-gen design compatibility. The device is developed under advanced process node and provides significant power efficiency.

The MV-CHP10160 supports flexible link bifurcation, with one x16, two x8, four x4, eight x2 and more combinations. The device takes PCIe base specification-compliant 100 MHz clock input and provides reference clock output to downstream devices. Common clock, SRIS, and SRNS are all supported clocking systems.

The MV-CHP10160 features advanced in- band and out-of-band diagnostics and telemetry functionality, supporting large-scale fleet management. It can be configured through SMBus/I3C or EEPROM/SPI flash for ease of adoption.

Block Diagram

Key Features

Features	Benefits
Standard and compatibility	• Compliant with PCI-SIG specifications for PCI Express® Gen-6.x/5/4/3/2/1 • Compliant with Compute Express Link™ 3.x/2.0/1.1 • Support cache-coherent application with low-latency mode • 32 bi-directional PCIe lanes; 16-lane upstream and 16-lane downstream • All lanes can operate at 64 GT/s, 32 GT/s, 16 GT/s, 8 GT/s, 5 GT/s, and 2.5 GT/s data rates • Flexible link bifurcation from 1 x16, 2 x8, 4 x4, and up to 8 x2 lanes per link • PCIe hot-add and hot-removal of end point devices independently on each link or partition
I/O performance	• First Bit Error Rate (FBER) better than 1E-6 • Support channel IL budget of >32 dB for PCIe 6, >36 dB for PCIe 5 at 16 GHz Nyquist frequency • Advanced equalization features support various channel topologies
Clocking	• Support Common Clock, SRIS, and SRNS • PCIe base specification compliant 100 MHz clock input • HCSL reference clock output to downstream devices
Management	• I2C/SMBus-compatible management interface with additional I3C features • On-chip voltage and thermal sensors
Design information	• Three external power rails • Package options for integrated DC-blocking capacitors • IBIS-AMI model for simulation • Device configuration through SMBus/I3C, EEPROM or SPI Flash • GPIO for quick indications of link status and functional status
Debug and diagnostics	• Advanced in-band and out-of-band diagnostics and telemetry features • IEEE 1149.6 AC-JTAG boundary scan • Embedded logic analyzer and history FIFO
Package characteristics	• MV-CHP10160: 8.9 mm × 22.8 mm HFETBGA package with minimum 0.5 mm ball pitch

Target Applications

• Motherboard PCIe/CXL trace-length extension
• Compute fabric of GPU/AI system
• PCIe riser card and backplane
• NVMe SSD storage and CXL disaggregated memory
• PCIe active electrical cable (PCIe AEC)