Product Brief

Marvell® Alaska® C 88X5243P

Quad 100G, 16 port 25G/10G/1G Ethernet Transceiver with 256 bit MACSec Encryption and Class C PTP Timestamping

Overview

The Marvell® Alaska® C 88X5243P is a fully integrated single chip Ethernet transceiver that performs IEEE 802.1AE MACSEc Encryption with 256 bit key and IEEE 1588v2 PTP Time Stamping functionality for four ports of 100 GbE or 40GbE, 8 ports of 50GbE, or 16 ports of 25 GbE, 10 GbE, 2.5 GbE, and 1 GbE. The device supports full-duplex transmission at all supported speeds, over a variety of media including optics, passive direct attach cables, and copper backplanes.

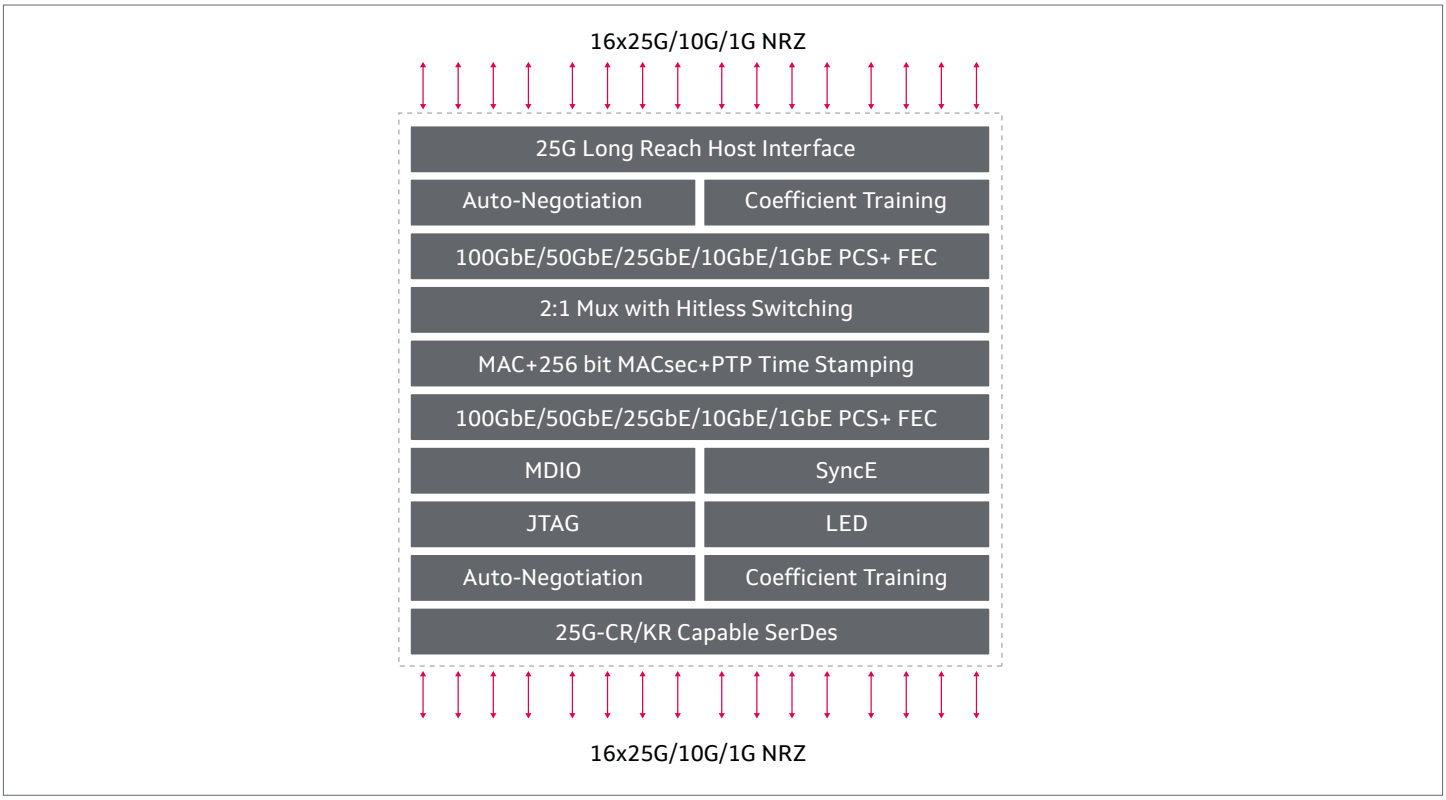
The PTP time stamping functionality in the device provides timing accuracy that meets the requirements of Class C profile, enabling high precision timing recovery required for wireless and carrier applications. The device provides recovered clock output for SyncE applications, with flexible clock source selection.

The X5243P integrates Long Reach dual mode SERDES, fully compliant to the IEEE electrical specifications for transmission over direct attach passive direct attach cables and copper backplanes. The device supports FEC generation and termination capabilities for all FEC types defined by 802.3by, 802.3bj, 802.3ba, 802.3ap and the 25 Gigabit Ethernet Consortium for 100 GbE, 50 GbE, 40 GbE, 25 GbE, and 10 GbE operation. The supported FEC types include Clause-91 (528, 514) RS-FEC, and FC (2212, 2080) FEC.

The device supports Auto-Negotiation and coefficient training protocol required by the IEEE 802.3 to support operation over KR backplanes and CR passive copper cables. The device has a fully symmetric architecture with Long Reach SerDes, FEC generation and termination functionality, and Auto-Negotiation and training capabilities on both host and line interfaces to provide complete system design flexibility.

The 88X5243P also supports 2:1 multiplexing functionality with hitless switching capability on the host interface to support applications requiring redundancy

Block Diagram



Key Features

Features	Benefits
Quad 100GbE, 16-port 25 GbE, 10 GbE, 1 GbE MACSec with 256bit key	· Enables encrypted links for all speeds from 1GbE up to 100GbE
IEEE 1588v2 PTP Timestamping that meets timing accuracy requirements for Class C PTP profile	· Accurate extraction of timing information for timing critical applications
Recovered clock for SyncE applications with flexible selection of clock	· Enables accurate transfer of clock over an Ethernet network
2:1 Mux on the host interface with hitless switching	· For applications requiring Active/Standby redundancy with seamless switchover
Long Reach host and line interface SERDES	· For driving passive direct attach copper (DAC) cables and backplanes
Fully symmetric architecture with FEC capability on host and line interfaces	· Flexibility to support a wide range of applications and system design choices
Support for IEEE Auto Negotiation and Training protocol	· Seamless interoperability with standards-compliant devices from other vendors
8x8 SerDes layer crossbar	· Enables board routing flexibility for the high speed I/Os
Ethernet packet and PRBS generation capabilities and eye monitoring capability on all high-speed interfaces	· Comprehensive debug capabilities

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