Product Brief

Marvell® Alaska® C 88X93160

Dual 800G, Quad 400G, Octal 200G, 16 port 100G Ethernet Transceiver with Passive Direct Attach Cable and Backplane Drive capabilities

Overview

The Marvell® Alaska® C 88X93160 is a fully integrated single chip Ethernet transceiver with Long Reach 100G PAM4 I/Os to drive passive direct attach cables (DAC) and backplanes. The device supports two ports of 800 GbE, four ports of 400 GbE, 8 ports of 200 GbE or 16 ports of 100GbE. The device is targeted to next generation high density networking solutions based on 100G serial electrical signaling.

The device also supports a variety of gearboxing modes to translate between 50G PAM4 and 100G PAM4 modes for 400GbE, 200GbE and 100 GbE, with the necessary FEC termination and regeneration capabilities.

The Long Reach Multi mode (112G PAM4, 56G PAM4 and 25G/10G NRZ) SerDes on the X93160 is fully compliant to the IEEE 802.3ck, 802.cd and 802.bj electrical specifications for transmission over passive direct attach (DAC) cables and copper backplanes.

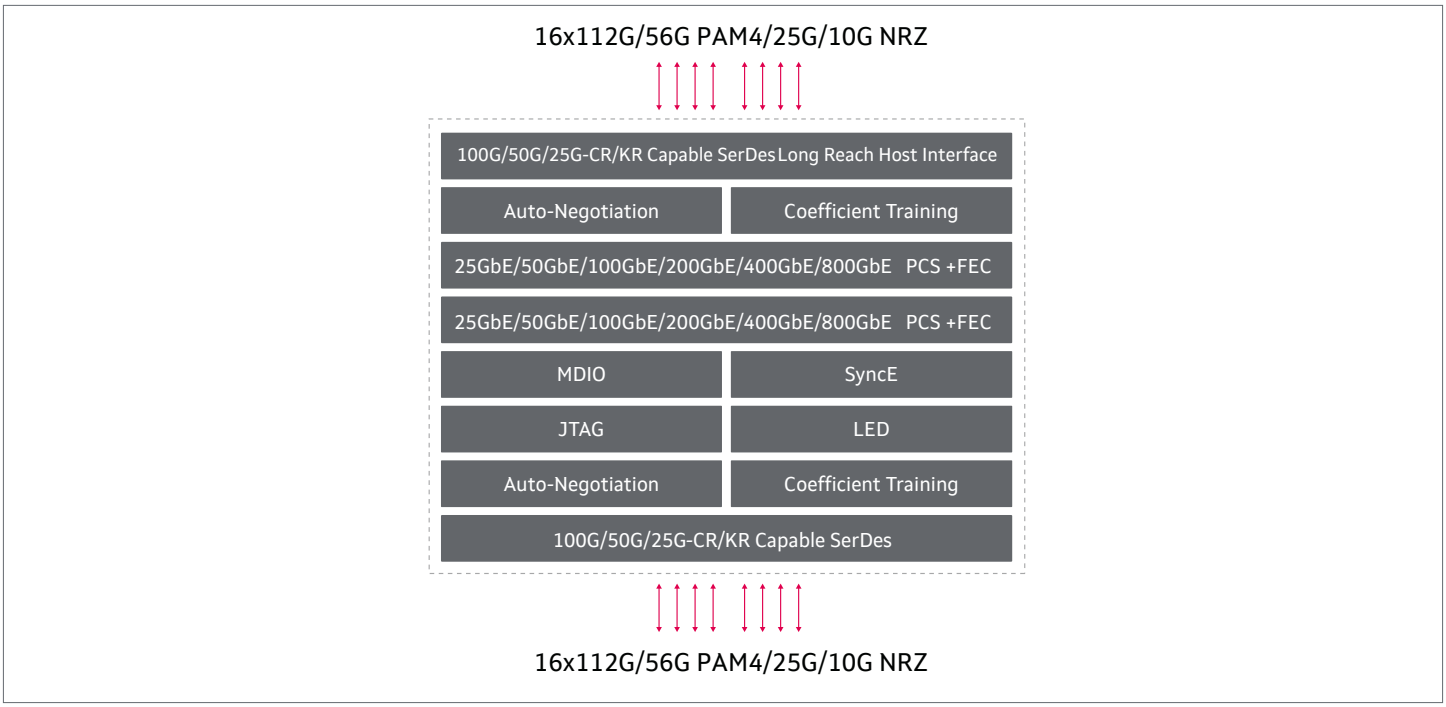
The device supports FEC generation and termination capabilities for all FEC types defined by IEEE 802.3ck, 802.3cd, 802.3by, 802.3bj, 802.3ba, 802.3ap and the 25 Gigabit Ethernet Consortium for 800GbE, 400GbE, 200 GbE, 100 GbE, 50 GbE, 40 GbE, 25 GbE, and 10 GbE operation. The supported FEC types include Clause-134 RS (544, 514), Clause-91 and Clause-108 RS (528, 514) RS-FEC, and FC (2212, 2080) FEC.

The device supports Auto-Negotiation and coefficient training protocol required by the IEEE 802.3 to support operation over KR backplanes and CR passive DAC cables. The device has a fully symmetric architecture with FEC generation and termination functionality, and Auto-Negotiation and training capabilities on both host and line interfaces to provide complete system design flexibility.

The device also includes a full 8x8 SerDes crossbar to support port multiplexing applications.

The 88X93160 is packaged in a 27mmx27mm FCBGA package with 0.9mm ball pitch.

Block Diagram



Key Features

Features	Benefits
Dual 800GbE, Quad 400GbE, Octal 200GbE, 16-port 100GbE	· Enables high density 100G serial based high density switching solutions
Dual 400GbE Gearbox for translation from 4x100G PAM4 to 8x50G PAM4	· Enables support of 50G PAM4 I/O based optics from switch ASICs with 100G PAM4 I/Os. Also enables support of new 100G-PAM4 optics with legacy switch ASICs
Long Reach host and line interface SerDes that exceed the IEEE 802.3ck requirements for CR & KR links	· For driving passive direct attach copper (DAC) cables and backplanes
Support for IEEE and Ethernet Consortium FECs for all Ethernet rates from 25GbE to 800GbE	· Ability to support a wide range of Ethernet rates and applications
Support for IEEE Auto Negotiation and Training protocol	· Seamless interoperability with standards-compliant devices from other vendors
Fully symmetric architecture with FEC capability on host and line interfaces	· Flexibility to support a wide range of applications and system design choices
Recovered clock for SyncE applications with flexible selection of clock	· Enables accurate transfer of clock over Ethernet networks
8x8 SerDes layer crossbar	· Enables Port Multiplexing applications
Ethernet packet and PRBS generation capabilities and eye monitoring capability on all high-speed interfaces	· Comprehensive test and debug capabilities

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To deliver the data infrastructure technology that connects the world, we're building solutions on the most powerful foundation: our partnerships with our customers. Trusted by the world's leading technology companies for 25 years, we move, store, process and secure the world's data with semiconductor solutions designed for our customers' current needs and future ambitions. Through a process of deep collaboration and transparency, we're ultimately changing the way tomorrow's enterprise, cloud, automotive, and carrier architectures transform—for the better.

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