Table of Contents

1. Overview

The Marvell Alaska 88E1510 and 88E1518 devices are physical layer devices containing a single 10/100/1000 Gigabit Ethernet transceiver. The transceiver implements the Ethernet physical layer portion of the 1000BASE-T, 100BASE-T, and 10BASE-T standards.

2. Features

- 10/100/1000BASE-T IEEE 802.3 compliant
- Supports RGMII host interfaces
- Supports Copper (10/100/1000M) Line interfaces
- Supports Four RGMII timing modes including integrated delays
- Supports LVCMOS I/O Standards on the RGMII interface
- Integrated MDI interface termination resistors that eliminate passive components
- Integrated switching Voltage regulators
- Energy Efficient Ethernet (EEE) – IEEE 802.3az-2010 compliant
- IEEE 1588 V2 Time Stamping support
- Synchronous Ethernet (SyncE) Clock recovery
- Three Loopback modes for diagnostics
- Downshift mode for two-pair cable installations
- Fully integrated digital adaptive equalizers, echo cancellers, and crosstalk cancellers
- Auto MDI/MDIX crossover at all speeds of operation
- Automatic polarity correction
- IEEE 802.3 compliant Auto-negotiation
- MDC/MDIO Management interface
- CRC checker, packet counter
- Packet generation
- Wake-on-Lan (WOL) event detection
- Advanced Virtual Cable Tester (VCT)
- Auto-calibration of MAC interface outputs
- Integrated Temperature sensor

3. Modes of Operation

The 88E1510/88E1518 device supports only RGMII to copper (10/100/1000BASE-T) mode.

4. Configuring the device

4.1 Hardware Strapping

After the de-assertion of RESETn, the device will be configured through CONFIG pin. This pin is used to configure 2 bits, per the bit mapping provided in Table 1.

Table 1: Two-bit Mapping

Pin	Bit 1, 0
VSS	00
LED[0]	01
LED[1]	10
LED[2]	Unused
VDDO	11

The 2 bits for the CONFIG pin are mapped as shown in Table 2.

Table 2: Configuration Mapping

Pin	CONFIG Bit 1	CONFIG Bit 0	Value Assignment
CONFIG	0	0	PHYAD[0] = 0 VDDO_LEVEL = 3.3V/1.8V
CONFIG	1	1	PHYAD[0] = 1 VDDO_LEVEL = 3.3V/1.8V
CONFIG	1	0	PHYAD[0] = 0 VDDO_LEVEL = 2.5V/1.8V
CONFIG	0	1	PHYAD[0] = 1 VDDO_LEVEL = 2.5V/1.8V

Note: For 88E1518, VDDO_LEVEL is fixed at 1.8V, hence the bit mapping for VDDO_LEVEL is ignored

At HardwareReset/Power up the device comes up in RGMII to Copper.

4.2 Default Jumper Settings

The 88E1510/88E1518 Demo Board should contain the following list of jumpers. These are the default settings from the factory and should not be changed unless instructed to do so. Please contact Marvell for more details.
Default Jumper setting are also specified in the schematic.

The following jumpers should be "IN":

JP12 JP14 JP25 JP26 JP27 JP29 JP30 JP31 JP32 JP33 JP37 JP39 JP40 JP41 JP42 JP43 JP44 JP45 JP46 JP49 JP50 JP51 JP52

For JP23, install: U1_RX_CLK, RX_CTRL, RX0, RX1, RX2, RX3.
For JP24, install: U1_TX_CLK, TX_CTRL, TX0, TX1, TX2, TX3.

Table 3: Jumper Settings

Jumper	1 - 2	2-3	3 - 4	5 - 6	7-8	9-10	11-12
JP2		X					
JP3	X		X				
JP11			X				
JP13				X			
JP23	X		X	X	X	X	X
JP24	X		X	X	X	X	X

The following jumpers should be "OUT":
JP4, JP5, JP36, JP38, JP47 JP48, JP53, JP55

5. Reference Clocks

This PHY accepts 25 MHz Crystal reference to the XTAL_IN & XTAL_OUT pins and oscillator input to the XTAL_IN pin.
The reference clock must be 25 MHz+/- 50ppm tolerance.

NOTE: The XTAL_IN pin is not 2.5V/3.3V tolerant. Use level shifters to convert a 2.5V/3.3V clock source to 1.8V clock.

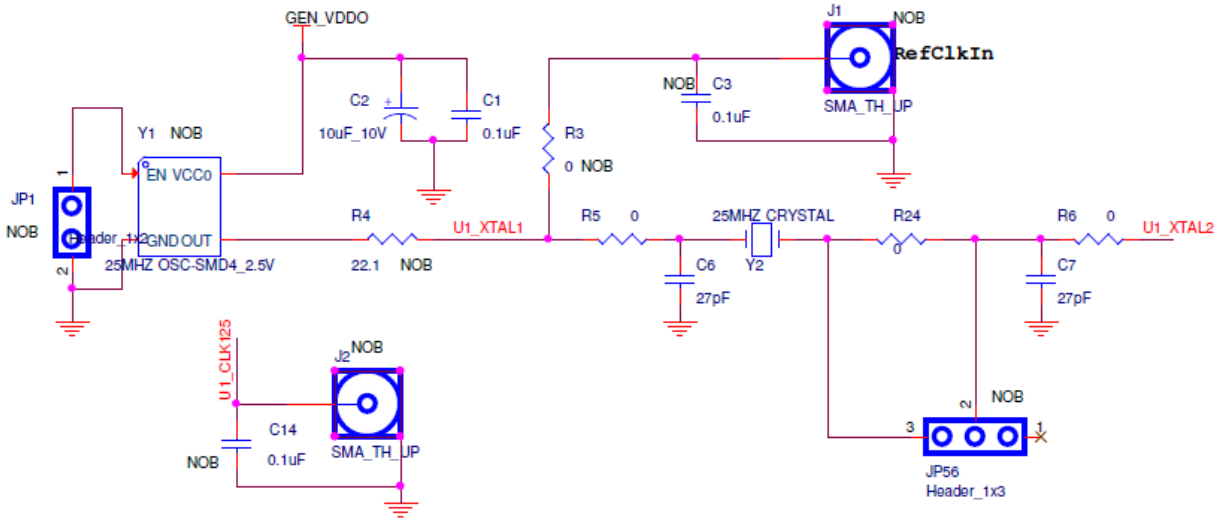

Figure 1: **XTAL_IN/OUT pin connections to crystal & Oscillator**

6. Power supplies

The device has built in switch cap regulator to support single rail operation from a 3.3V source. These internal regulators generate 1.8V & 1.0V. If the internal regulators are not used then external 1.8V and 1.0V supply are needed.
The VDDO supply can run at 2.5V or 3.3V for the 88E1510 and 1.8V for 88E1518.

When internal regulators are used both 1.0V and 1.8V regulators must be used, supply 1.0V internally and 1.8V externally (or vice versa) is not supported.

6.1 Internal regulator selection

The internal regulators can be enabled by connecting REGCAP1 & REGCAP2 pins to each other via a 220nF capacitor. The AVDD18_OUT and DVDD_OUT will output the 1.8V and 1.0V required for the PHY.
NOTE: The regulator outputs must not be used to power other devices.

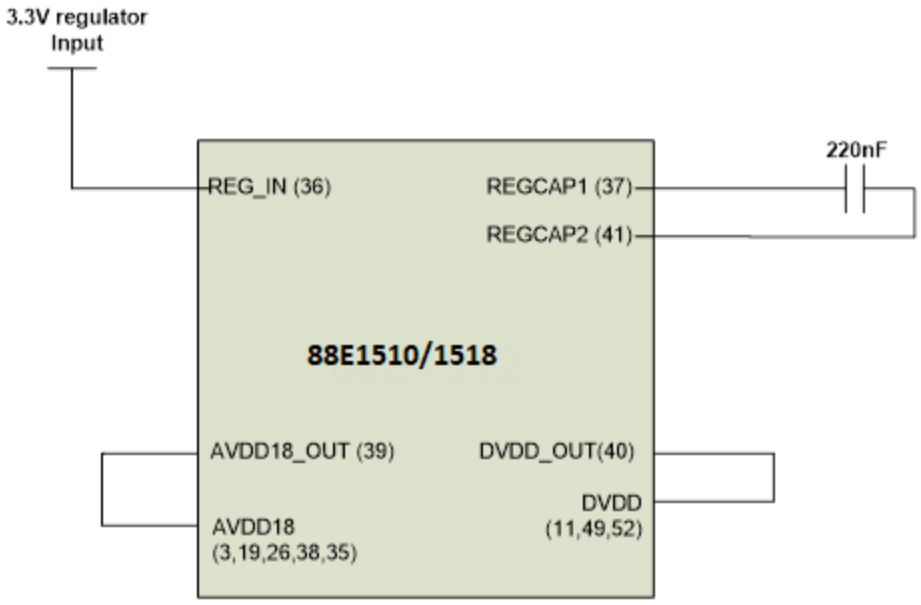

Figure 2: 88E1510/88E1518 Internal Regulator Connections

7. Bringing up the device

7.1 Hardware requirements

- Verify all the supplies are ramped up and stable following the datasheet RESETn timing. The supply noise must be <50mVp-p.
- Ensure the reference clock is toggling and stable (no excessive jitter).
- De-assert the RESET_n. Follow the reset timing requirement provided in datasheet.

7.2 Software requirements

- Ensure the MDC/MDIO interface Clause-22 protocol is implemented correctly.
- After the device powers up, the PHY registers should be accessible
- Marvell provides an API function call for this part, which can be incorporated into the customer's software. These API's can be used to configure the PHY via software.

7.3 MDIO Register Description

IEEE defines only a 32 register address space for the PHY. In order to extend the available register address space, a paging mechanism is used. Register 22 [7:0] are used to specify the page. There is no paging for Register 22.
In this document, short hand is used to specify the registers take the form register_page.bit:bit , register_page.bit, register.bit:bit or register.bit

Example:
Register 17 page 0 bit 15 to 14 is specified as 17_0.15:14
Register 17 page 0 bit 10 is specified as 17_0.10
Register 20 bit 15 is preseneted as 20.15

8. Sample Applications

8.1 RGMII to copper

The device by default comes up in RGMII to Copper.

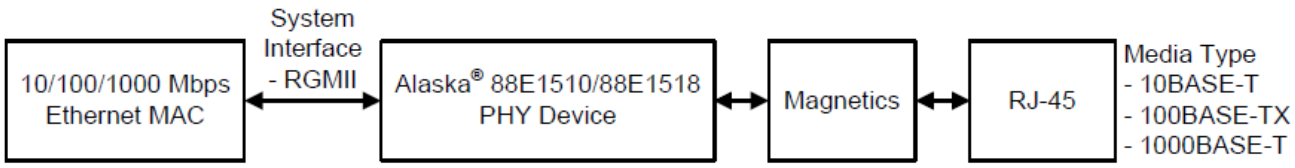

Figure 3: RGMII to Copper Device Application

Use the following register writes to change the mode:

Write Reg 22 = 0x12 // Change the page to 18 (hex 0x12)
Write Reg 20.2:0 = "000" // Go to "RGMII to Copper" mode
Write Reg 20.15 = 1 // Soft-reset for the Mode change to take effect.
Write Reg 22 = 0x00

8.1.1 Setting RGMII Delays

RGMII interface by spec needs the clock delayed with respect to the data to ensure correct sampling of the data. This PHY can incorporate the delay internally on both TX & RX by setting few registers. Depending on the customers application they can enable the delays in the PHY, in the MAC or on the trace. By default the RGMII delays are enabled in the PHY. To change the delay settings use the following register writes below.

Write Reg 22 = 0x2
Write Reg 21 = xxxx xxxx x00x xxxx // Bit 5 = Rx timing control; Bit 4 = Tx timing control
Write Reg 0 = 0x9140

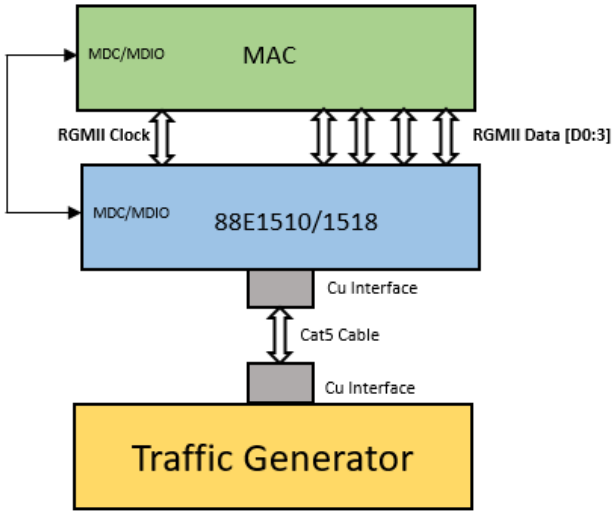

Figure 4: Block diagram showing RGMII to Copper on 88E1510/88E1518

8.1.2 Testing

- Ensure the RGMII interface is properly connected to the MAC with RGMII delays enabled.
- Connect the copper port to Traffic generator.
- Make sure the copper link comes up in the PHY
  - Check Link status
    - **Read Reg 17_0.10** // bit 10 provides real time link status
    - **Read Reg 17_0.15:14** // these bits provide Link speed
- Once the Copper link is established, send traffic from traffic Generator and see if the MAC received the packets.