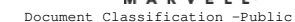


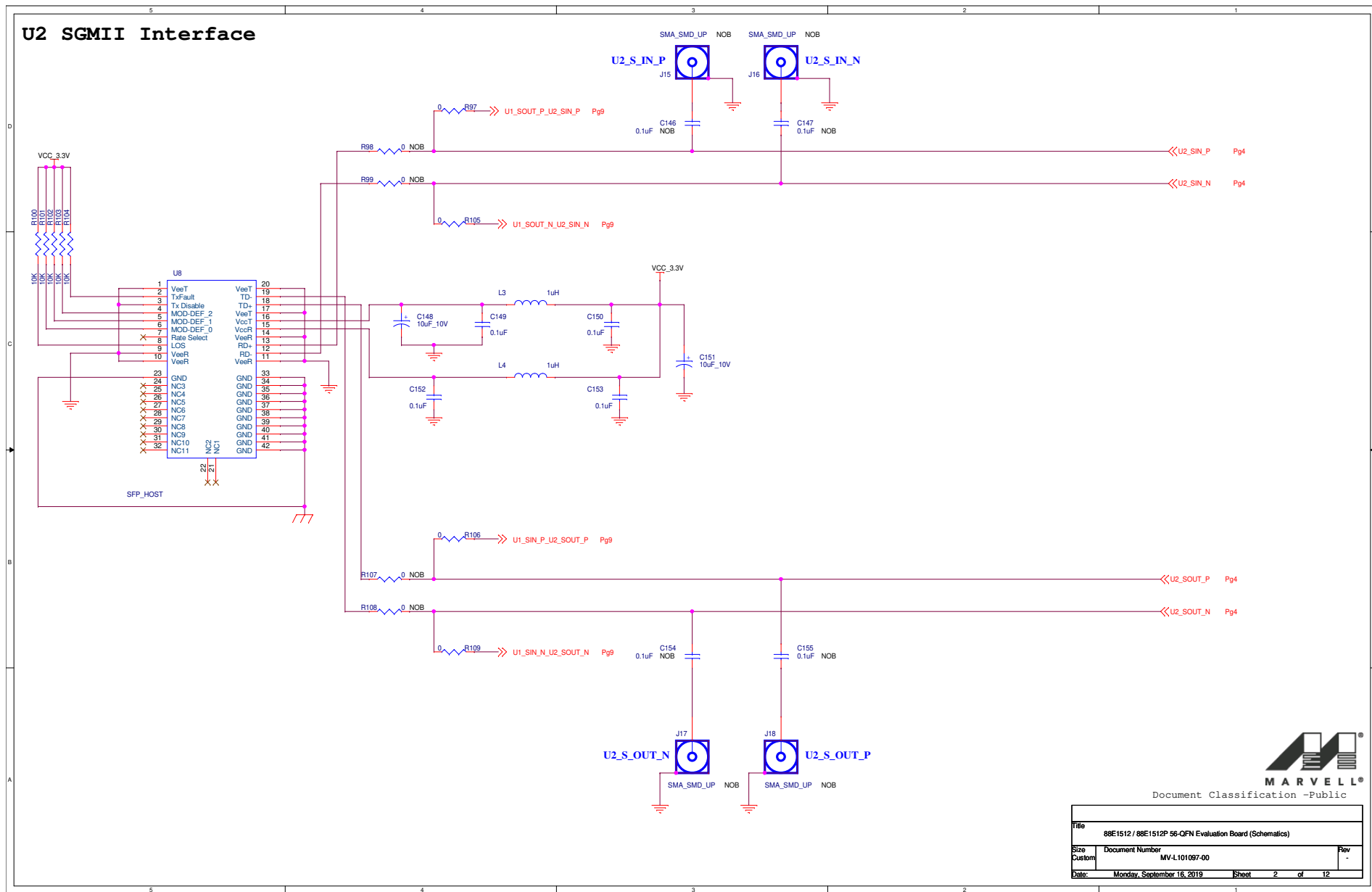
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Revision History		
DATE	REVISION	DESCRIPTION
01/11/2016	-	Initial release



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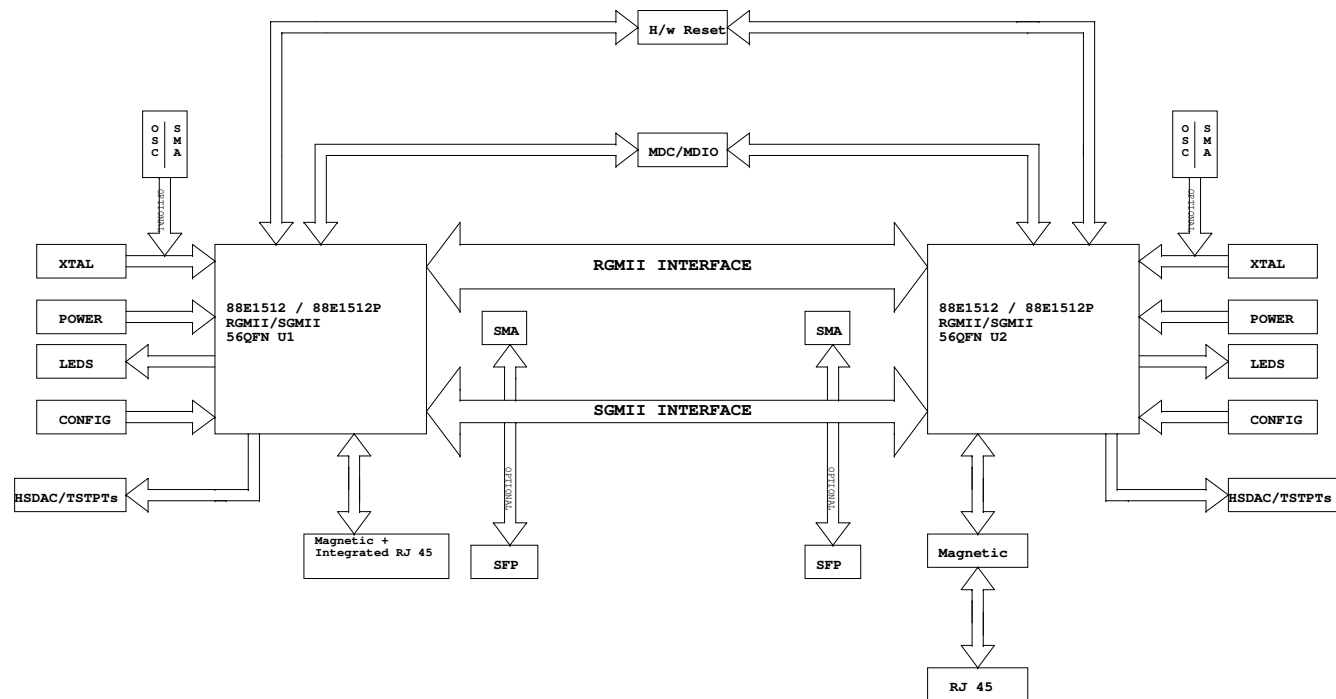
U2 SGMII Interface



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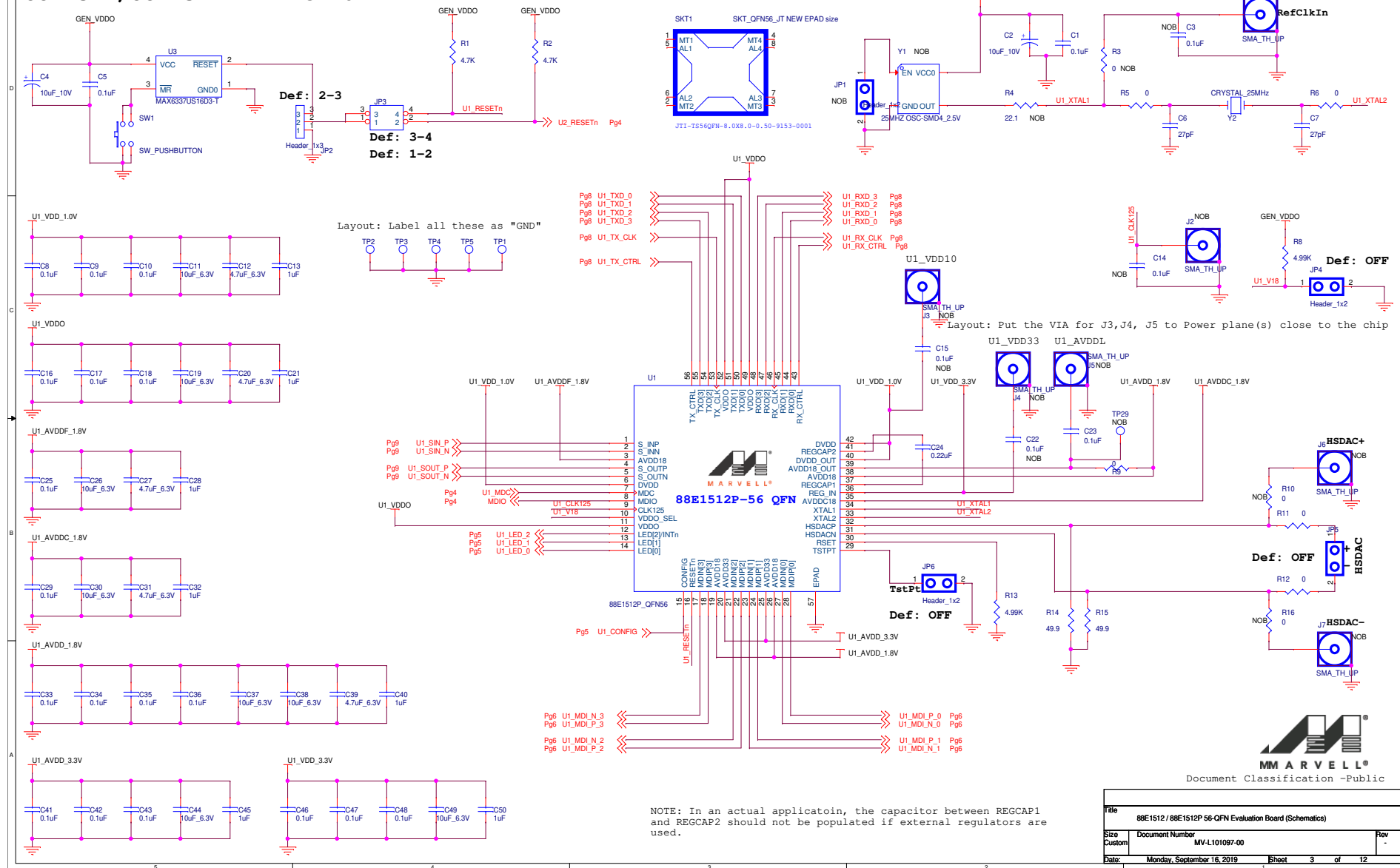
TOP LEVEL BLOCK DIAGRAM



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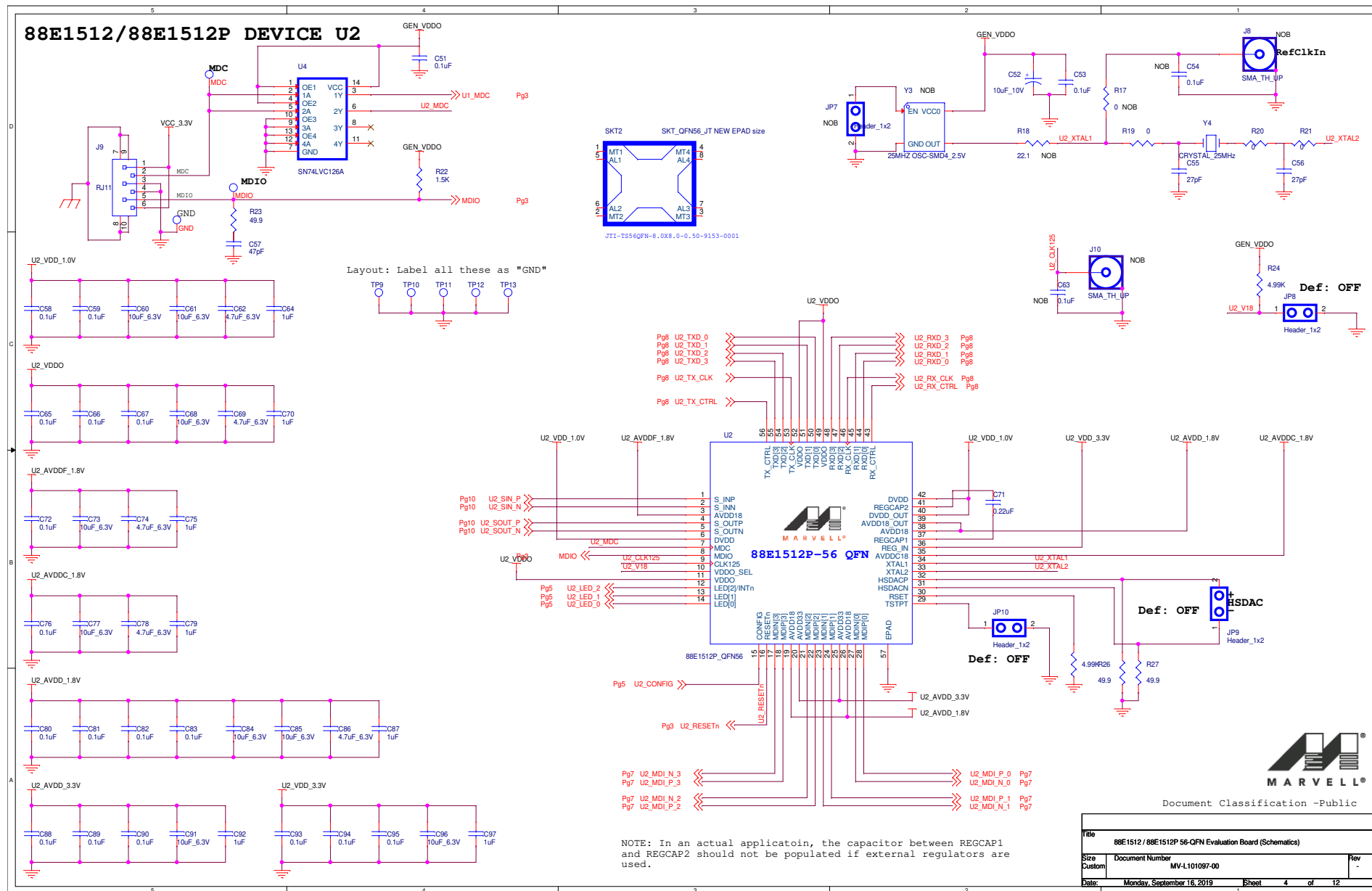
88E1512/88E1512P DEVICE U1



NOTE: In an actual applicatoin, the capacitor between REGCAP1 and REGCAP2 should not be populated if external regulators are used.

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88E1512/88E1512P DEVICE U2



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LEDs-CONFIGURATION

LED 0
LED GREEN

LED 1
LED GREEN

LED 2
LED GREEN

Remove JP56 and JP57 after PHY is configured when using PTP function.

Def: ON
JP56 Header_1x2
R163
0 NOB
U1_TRIG_GEN

GEN_VDDO
R145 4.7K
JP11 Header_2x4
R146 4.7K
Def: ON
JP57 Header_1x2
U1_CONFIG Pg3

Def: ON
JP12 Header_1x2

LED 0
LED GREEN

LED 1
LED GREEN

LED 2
LED GREEN

Remove JP54 and JP58 after PHY is configured when using PTP function.

Def: ON
JP54 Header_1x2
R164
0 NOB
U2_TRIG_GEN

GEN_VDDO
R148 4.7K
JP13 Header_2x4
R147 4.7K
Def: ON
JP58 Header_1x2
U2_CONFIG Pg4

Def: ON
JP14 Header_1x2

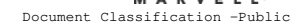
NOTE: The PTP clock should not be driven until the device is stabilized and the hardware configuraiton has completed.

U1_PTP_CLK
R149 0 NOB
NOB SMA_TH_UP J28

U2_PTP_CLK
R150 0 NOB
NOB SMA_TH_UP J29

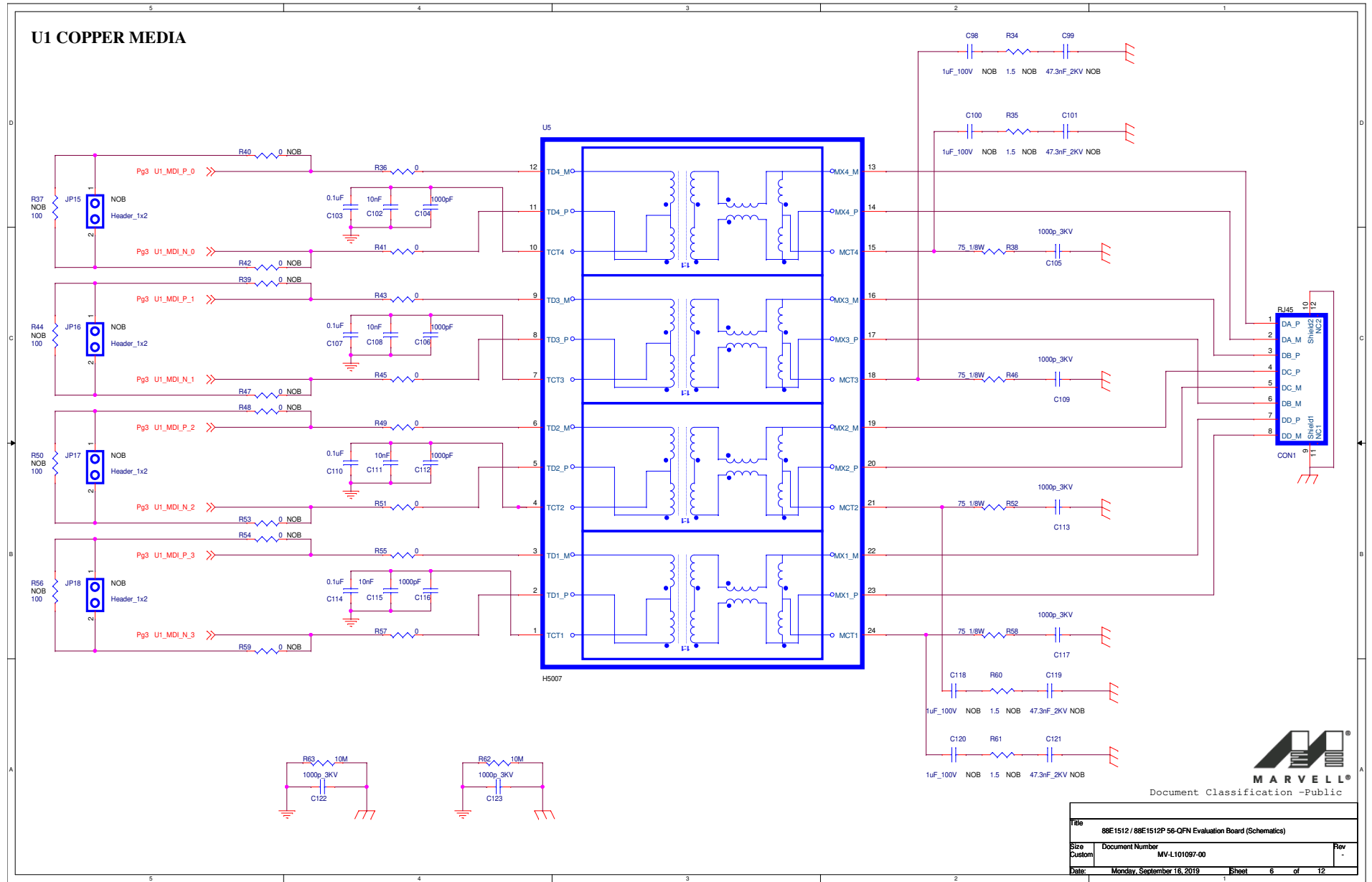
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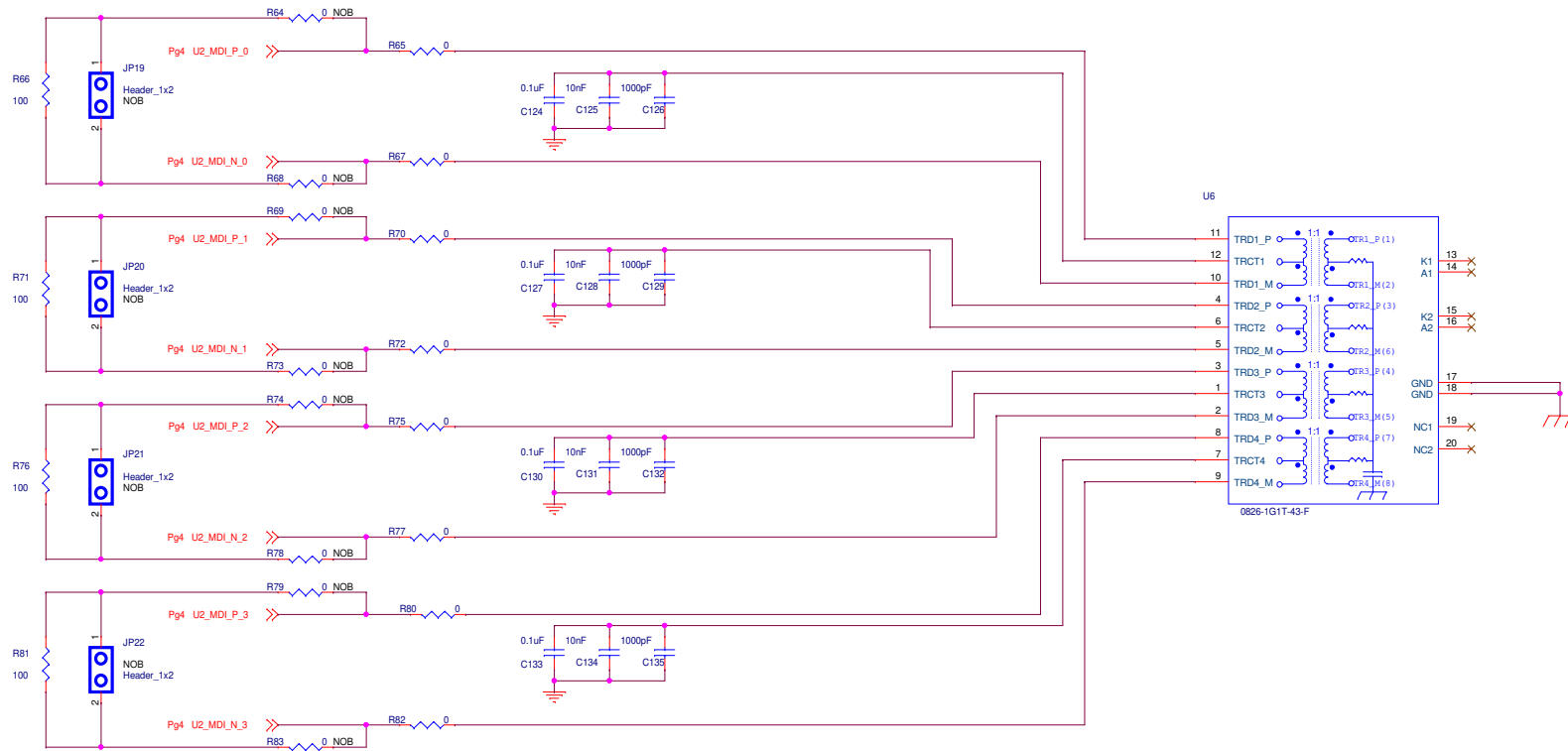
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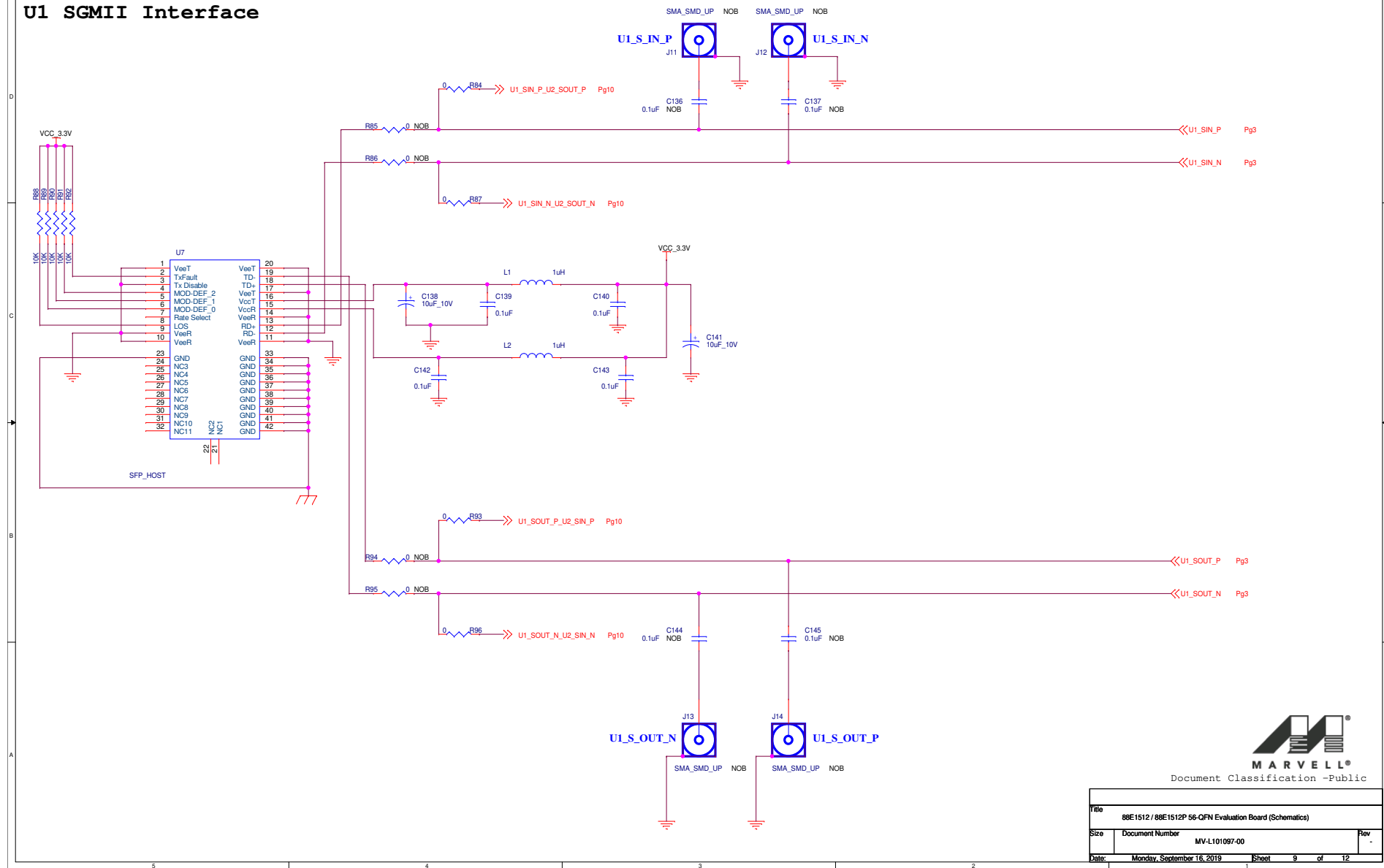
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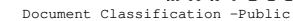
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U1 SGMII Interface



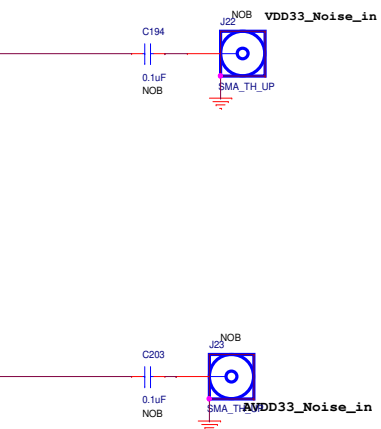
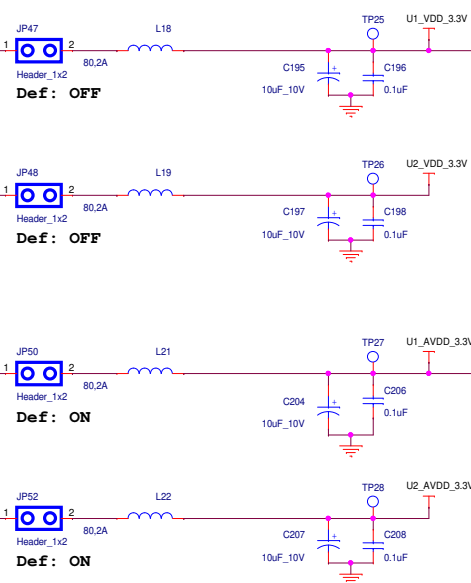
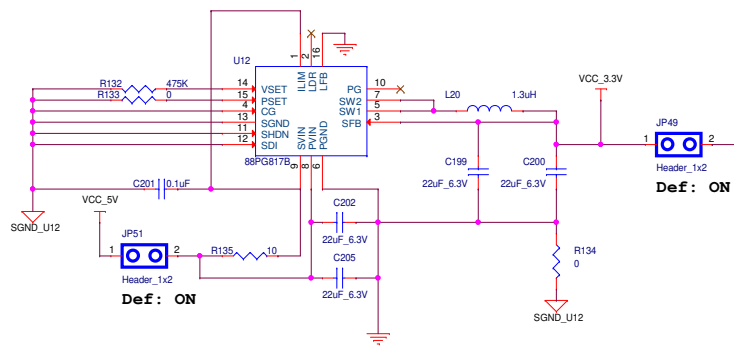
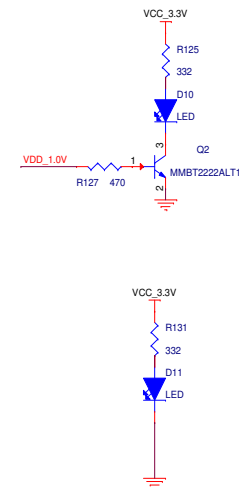
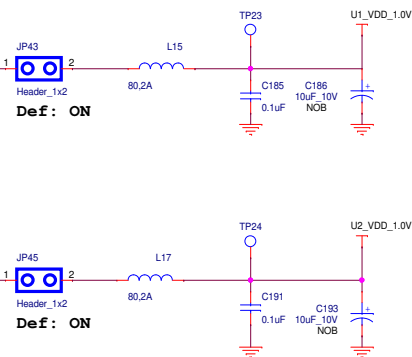
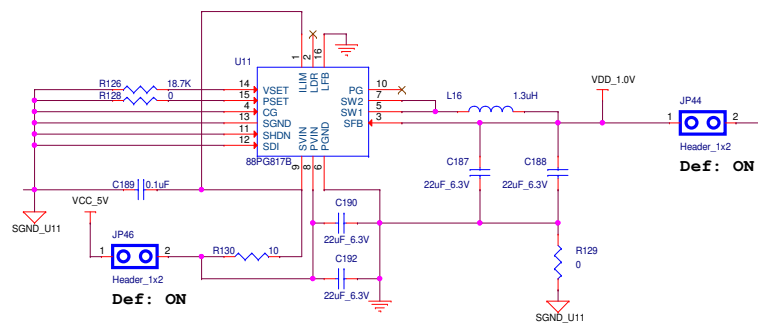
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SUPPLIES PART 2



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