Product Brief

Marvell® ALASKA C 88X7120

Dual 400G, Quad 200G, Octal 100G, 16 port 50G/25G Ethernet Transceiver

Overview

The Marvell Alaska C 88X7120 is a fully integrated single chip Ethernet transceiver that performs retiming functionality for two ports of 400GbE, and PHY/retiming functionality for four ports of 200GbE, 8 ports of 100GbE or 16 ports of 50GbE, 25GbE, 10GbE and 1GbE. The device supports full duplex transmission at all supported speeds, over a variety of media including optics, passive direct attach cables and copper backplanes.

The device also supports the gearboxing modes to translate between NRZ and PAM4 modes for 50G and 100G Ethernet, with the necessary FEC termination and regeneration required to translate between NRZ and PAM4 operation.

The 88X7120 integrates Long Reach dual mode (PAM4 and NRZ) SerDes, fully compliant to the IEEE electrical specifi cations for transmission over passive direct attach 802.3bs, cables and copper backplanes.

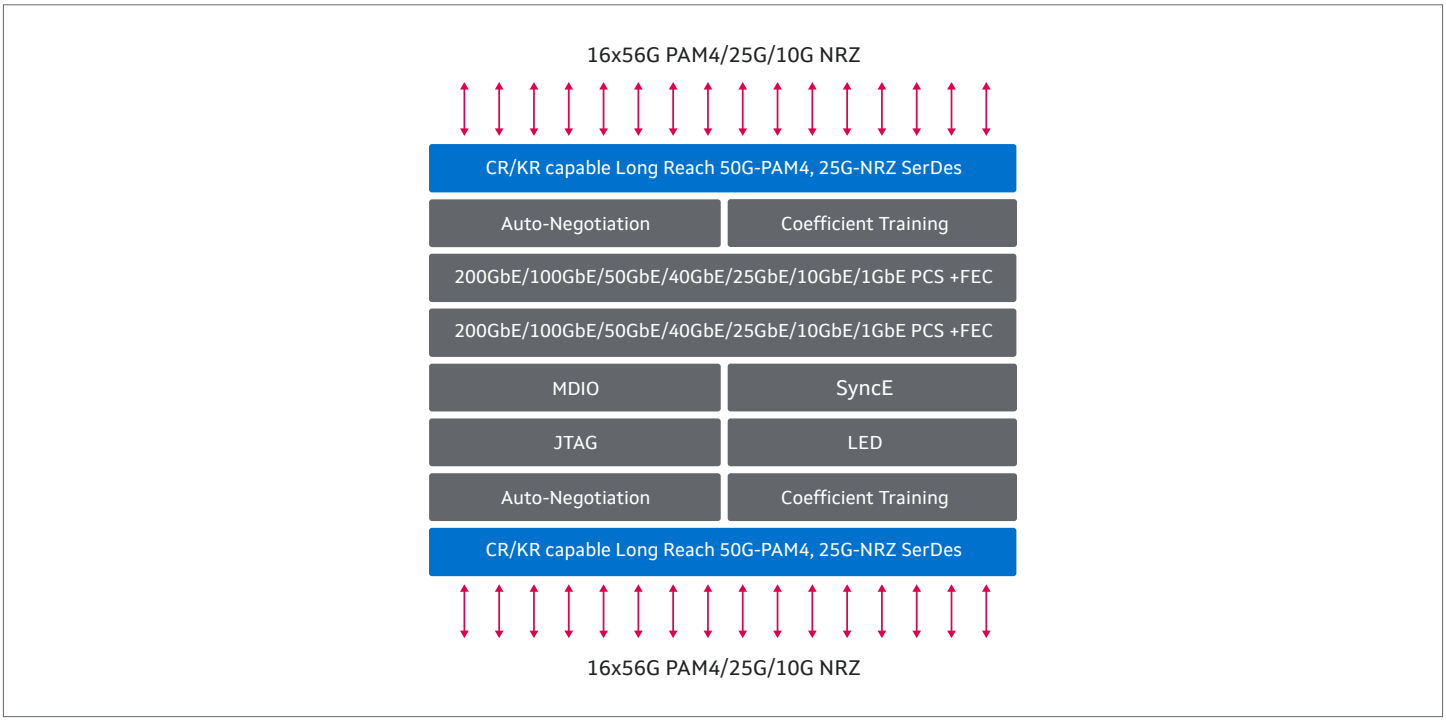
The device supports FEC generation and termination capabilities for all FEC types defined by IEEE 802.3bs, 802.3cd, 802.3bj, 802.3ba, 802.3by and 25G consortium for 200GbE, 100GbE, 50GbE, 40GbE, and 25GbE.

The supported FEC types include Clause-134 RS(544,514), FEC Clause-91 and Clause-108 RS(528,514) FEC and FC(2212,2080) FEC. This device also supports Auto-negotiation and coeffi cient training protocol required by the IEEE 802.3 to support operation over KR backplanes and CR passive copper cables.

The 88X7120 has a fully symmetric architecture with Long Reach serdes, FEC generation and termination functionality, and Autonegotiation and training capabilities on both host and line interfaces to provide complete system design fl exibility.

It can also operate as a 16 port protocol agnostic transparent retimer in which the digital logic associated with the PCS and FEC functionalities are bypassed, and powered down for a low latency, low power operation. The transparent mode is support for both PAM4 and NRZ signaling.

Block Diagram



Key Features

Features	Benefits
Dual 400G Ethernet Retimer, Quad 200G PHY/Retimer	• Enables the new high density QSFP-DD and OSFP form factors targeted to 400GbE applications in datacenters
16 port 50GbE, 25GbE, 10GbE, 1GbE PHY/Retimer	• Ideal for high density Top of Rack switches supporting 50G/25G connectivity to servers
Quad 100GbE Gearbox for translation from 802.3bj 4x25G NRZ to 802.3cd 2x50G PAM4	• Enables support of 4x25G optics from switch ASICs with 2x50G PAM4 I/Os. • Also enables support of new 50G optics with older switch ASICs
Low latency 16 channel transparent retiming functionality in PAM4 and NRZ modes	• For low latency retiming applications
Long Reach Host and Line interface serdes	• For driving passive Direct Attach Copper (DAC) cables, and backplanes
Fully symmetric architecture with FEC capability on host and line interfaces	• Flexibility to support wide range of applications and system design choices
Support for IEEE Auto-negotiation and Training protocol	• Seamless interoperability with standards compliant devices from other vendors
Ethernet Packet and PRBS generation capabilities, and eye monitoring capability on all high speed interfaces	• Comprehensive debug capabilities

Target Applications

- 100G, 50G, 25G Top of Rack Datacenter switches
- 400G and 200G Ethernet line cards

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